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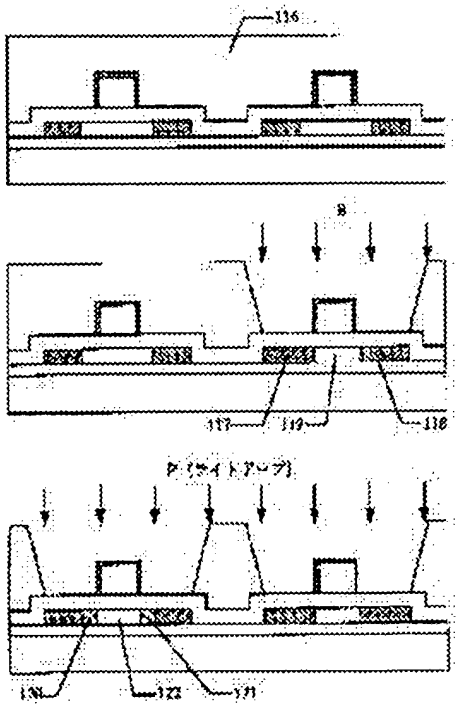
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE OF THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To eliminate a resist mask for doping and reduce organic contamination of a semiconductor device, by using an interlayer insulating film as a mask in a doping step.

SOLUTION: An interlayer insulating film 116 is formed to cover a gate insulating film and a gate electrode formed on an insulating substrate. Next, the interlayer insulating film 116 is patterned to open a hole above a semiconductor island region to be a P-channel transistor. Then, boron ions are implanted by using the interlayer insulating film 116 as a mask and the conductivity type of the impurity region is inverted, thus forming p-type impurity regions 117 and 118 and forming a channel forming region 119 of the P-channel transistor. Moreover, a hole is opened above a semiconductor island region to be an N- channel transistor and phosphorus is implanted, thus forming n-type impurity regions 120 and 121 and forming a channel forming region 122 of the N-channel transistor.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to an insulated gate field effect transistor (only henceforth a transistor), and its production approach. It is related with the semiconductor device which has a P channel mold transistor and an N channel mold transistor on the same substrate especially, and its production approach. It is related especially with simplification of a making process.
[0002]
[Description of the Prior Art] Many semiconductor devices which have the complementary transistor which consists of a P channel mold transistor and an N channel mold transistor are on the same substrates, such as IC. Moreover, that by which the circuit for driving a liquid crystal display and a liquid crystal display was formed on the insulating substrate also comes to be made from recent years, and the circuit for driving a liquid crystal display has the complementary transistor.
[0003] In case a P channel mold transistor and an N channel mold transistor are formed on the same substrate, the impurity doped in a semi-conductor layer must be had good control of striking in any direction with a P channel mold transistor and an N channel mold transistor.
[0004] A mask is carried out in this case, for example, the semi-conductor layer top which serves as a P channel mold transistor first, and Lynn is poured in into the semi-conductor layer used as an N channel mold transistor. Then, said mask is removed, a mask is shortly made the semi-conductor layer used as an N channel mold transistor, and boron is poured in into the semi-conductor layer used as a P channel mold transistor. Thus, at least two masks are required to have good control of striking an impurity in any direction.
[0005] On the other hand, the mask for doping is reduced to one sheet, and the process which simplified the making process of a complementary transistor is proposed. The outline of this process is shown below. In drawing 3 , the semi-conductor island fields 303 and 304 are formed after forming the substrate film 302 on an insulating substrate 301. Gate dielectric film 305 is formed after that. And the gate electrodes 306 and 307 are formed on gate dielectric film 305. In this way, the condition of drawing 3 (A) is acquired.
[0006] Next, Lynn (P) is poured in into all the semi-conductor island fields 303 and 304 by using the gate electrodes 306 and 307 as a mask. In this way, the impurity ranges 308-311 of N type are formed. (Drawing 3 (B))
[0007] Then, a mask 312 is formed on the semi-conductor island field 303 used as an N channel mold transistor. A mask 312 is formed by the lithography technique of using a resist. And boron (B) is poured in all over the semi-conductor island field 304 used as a P channel mold transistor. At this time, the dose of boron is made [more] than the dose of drawing 3 (Lynn (P in B)). If it carries out like this, impurity ranges 310 and 311 will be reversed in p mold. (Drawing 3 (C))
[0008] And a mask 312 (it consists of a resist etc.) is removed, and an interlayer insulation film 313 is formed. Next, a contact hole is formed in an interlayer insulation film 313 and gate dielectric film 305, and the source drain electrodes 314-316 are formed. In this way, an N channel mold transistor and a P channel mold transistor are obtained on the same substrate. (Drawing 4 (D))
[0009]
[Problem(s) to be Solved by the Invention] Thus, generally a resist is used for the mask for doping. The lithography technique using a resist is very useful to micro processing in manufacture of semiconductor devices, such as LSI.
[0010] However, since it consists of the organic substance, after a resist removes a resist, the probability for residual organic substance contamination to occur is very high [a resist]. Moreover, in a resist removal process, there is also contamination by the heavy metal from an etching system. Furthermore, since a substrate is heated by the elevated

temperature at a doping process, a resist hardens with the heat, it becomes impossible that it is hard to take a resist at a next resist removal process, and there is also a problem that productivity falls. Moreover, since ashing is carried out by long duration, ******, etc., the damage by the plasma will be received.

[0011] Therefore, the process which does not use a resist in a doping process is searched for. This invention aims at losing the mask for doping from a making process, without complicating a making process.

[0012]

[Means for Solving the Problem] The main point of invention indicated on these specifications is characterized by using an interlayer insulation film as a mask for doping in the production approach of a semiconductor device of having a P channel mold transistor and an N channel mold transistor, on the same substrate.

[0013] The 1st of this invention is a process which forms the thin film transistor of a top gate mold on an insulating substrate. Namely, the process which forms at least two semi-conductor island fields on an insulating substrate, The process which forms gate dielectric film on said semi-conductor island field, and the process which forms a gate electrode on said gate dielectric film, The process which pours in the 1st impurity all over said semi-conductor island field by using said gate electrode as a mask, The process which covers said gate dielectric film and said gate electrode, and forms an interlayer insulation film, Patterning of said interlayer insulation film is carried out, and it is characterized by having the process which exposes at least one of said gate electrodes, and the process which pours in the 2nd impurity all over the semi-conductor island field under said exposed gate electrode by using said gate electrode and said interlayer insulation film as a mask.

[0014] The 2nd of this invention is a process which forms a transistor in a semi-conductor substrate. Namely, the process which forms gate dielectric film on a semi-conductor substrate and the process which forms at least two gate electrodes on said gate dielectric film, The process which pours in the 1st impurity into said semi-conductor by using said gate electrode as a mask, The process which covers said gate dielectric film and said gate electrode, and forms an interlayer insulation film, Patterning of said interlayer insulation film is carried out, and it is characterized by having the process which exposes at least one of said gate electrodes, and the process which pours in the 2nd impurity into said semi-conductor by using said gate electrode and said interlayer insulation film as a mask.

[0015] The 3rd of this invention is a process which forms the transistor of a bottom gate mold. Namely, the process which forms at least two gate electrodes on an insulating substrate, The process which forms gate dielectric film on said gate electrode, and the process which forms at least two semi-conductor layers on said gate dielectric film, The process which forms an interlayer insulation film on said semi-conductor layer, and the process which carries out patterning of said interlayer insulation film, and exposes a part of at least one semi-conductor layer among said semi-conductor layers, The process which carries out patterning of said interlayer insulation film to the process which pours in the 1st impurity into said exposed semi-conductor layer by using said interlayer insulation film as a mask, and exposes a part of semi-conductor layer of others [layer / said / which was exposed / semi-conductor], It is characterized by having the process which pours in the 2nd impurity into said semi-conductor layer by using said interlayer insulation film as a mask.

[0016] Moreover, the semiconductor device produced at the process of this invention has the following descriptions. Namely, it sets to the semiconductor device which has at least one P channel mold transistor and at least one N channel mold transistor. Said P channel mold transistor and said N channel mold transistor, respectively A channel formation field, a source field, and a drain field, The gate electrode formed in the neighborhood of said channel formation field through gate dielectric film, The source wiring electrically connected to said source field, and drain wiring electrically connected to said drain field, It has the interlayer insulation film formed in the bottom of said source wiring and said drain wiring. To said interlayer insulation film It is characterized by adding the same impurity as the impurity added by the source field and drain field of said P channel mold transistor or said N channel mold transistor.

[0017] Furthermore, in the above-mentioned configuration, concentration of the impurity added by said interlayer insulation film is characterized by being the distribution which has inclination in the direction of thickness of said interlayer insulation film. Moreover, thickness of said interlayer insulation film is characterized by being 0.3 micrometers or more. Furthermore, it is characterized by said interlayer insulation film consisting of an inorganic substance.

[0018] Otherwise, an interlayer insulation film may be made two-layer. Namely, it sets to the semiconductor device which has at least one P channel mold transistor and at least one N channel mold transistor. Said P channel mold transistor and said N channel mold transistor, respectively A channel formation field; a source field, and a drain field, The gate electrode formed in the neighborhood of said channel formation field through gate dielectric film, Gate wiring electrically connected to said gate electrode, and the source wiring electrically connected to said source field, Drain wiring electrically connected to said drain field, and the 1st interlayer insulation film formed on said gate wiring, It has

said source wiring or said drain wiring, and the 2nd interlayer insulation film formed between said 1st interlayer insulation film. To said 1st interlayer insulation film It is characterized by adding the same impurity as the impurity added by the source field and drain field of said P channel mold transistor or said N channel mold transistor.
[0019] It is characterized by furthermore the concentration of the impurity added by said 1st interlayer insulation film being the distribution which has inclination in the direction of thickness of said interlayer insulation film in the above-mentioned configuration. Moreover, thickness of said 1st interlayer insulation film is characterized by being 0.3 micrometers or more. Furthermore, it is characterized by said interlayer insulation film consisting of an inorganic substance.
[0020] Moreover, it sets as other descriptions to the semiconductor device which has at least one P channel mold transistor and at least one N channel mold transistor. Said P channel mold transistor and said N channel mold transistor, respectively A channel formation field, a source field, and a drain field, The gate electrode formed in the neighborhood of said channel formation field through gate dielectric film, The source wiring connected to the source electrode connected to said source field at said source electrode, It has the drain electrode connected to said drain field, and the interlayer insulation film formed in the bottom of drain wiring connected to said drain electrode, said source wiring, or said drain wiring. To said gate dielectric film Said interlayer insulation film, It is characterized by a level difference being in the neighborhood said source electrode or a drain electrode touches.
[0021] As other descriptions, furthermore, at least one P channel mold transistor, Gate wiring electrically connected to the gate electrode of at least one N channel mold transistor, and said P channel mold transistor or said N channel mold transistor, The source wiring electrically connected to the source field of said P channel mold transistor or said N channel mold transistor, Drain wiring electrically connected to the drain field of said P channel mold transistor or said N channel mold transistor, It has the interlayer insulation film prepared between said gate wiring, and said source wiring or said drain wiring, and is characterized by carrying out opening of said interlayer insulation film on said P channel mold transistor and said N channel mold transistor.
[0022] Moreover, in the two above-mentioned configurations, it is characterized by the same impurity as the impurity added by the source field and drain field of said P channel mold transistor or said N channel mold transistor being added by said interlayer insulation film. Furthermore, concentration of the impurity added by said interlayer insulation film is characterized by being the distribution which has inclination in the direction of thickness of said interlayer insulation film. Moreover, thickness of said interlayer insulation film is characterized by being 0.3 micrometers or more. Furthermore, it is characterized by said interlayer insulation film consisting of an inorganic substance.
[0023] Furthermore, it not only uses an interlayer insulation film as the mask for doping, but it can use as a spacer for LDD (Lightly Doped Drain) field formation as other invention. Namely, the process which forms a semi-conductor island field on an insulating substrate as the production approach of a thin film transistor, The process which forms gate dielectric film on said semi-conductor island field, and the process which forms a gate electrode on said gate dielectric film, The process which pours in a low-concentration impurity all over said semi-conductor island field by using said gate electrode as a mask, The process which covers said gate dielectric film and said gate electrode, and forms an interlayer insulation film, It is characterized by having the process which etches said interlayer insulation film and forms a spacer in the side face of a gate electrode, and the process which pours in a high-concentration impurity all over said semi-conductor island field by using said gate electrode and said spacer as a mask.
[0024] Moreover, the transistor formed on a semi-conductor substrate is producible similarly. Namely, the process which forms gate dielectric film on a semi-conductor substrate and the process which forms a gate electrode on said gate dielectric film, The process which pours in a low-concentration impurity into said semi-conductor by using said gate electrode as a mask, The process which covers said gate dielectric film and said gate electrode, and forms an interlayer insulation film, It is characterized by having the process which etches said interlayer insulation film and forms a spacer in the side face of a gate electrode, and the process which pours in a high-concentration impurity into said semi-conductor by using said gate electrode and said spacer as a mask.
[0025]
[Embodiment of the Invention] In the process indicated by the 1st of this invention thru/or the 2nd, the interlayer insulation film is used as a mask at the time of doping the 2nd impurity. Moreover, at the process indicated by the 3rd of this invention, it is used as a mask at the time of doping the 1st thru/or the 2nd impurity.
[0026] Since there are usually 0.3 micrometers or more of thickness of an interlayer insulation film, a function can fully be achieved as an electric shielding mask in the case of doping of an impurity. Moreover, the operation as most important intersection spacer of vertical wiring of interlayer insulation film original does not have being spoiled by this invention. Furthermore, if another interlayer insulation film is formed on an interlayer insulation film, the insulation during vertical wiring will go up. Thus, the mask for doping can be lost from a making process by this invention,

without complicating a making process.
[0027] Furthermore, in the etching process for doping, since etching for contact hole formation of a source field and a drain field is also performed to coincidence, the making process of this invention can simplify a process.
[0028] Moreover, an interlayer insulation film can also be used as a LDD spacer of the side face of a gate electrode. If this process is used, since it is not necessary to form the film for spacers and a contact hole can also be further formed in spacer formation and coincidence, a process can be simplified.
[0029]
[Example]
[Example 1] In this example, it is the production approach of the complementary-type thin film transistor of a top gate mold. The making process Fig. of this example is shown in drawing 1 and drawing 2 . Suppose that an N channel mold transistor is formed in left-hand side, and a P channel mold transistor is formed in right-hand side in drawing 1 and drawing 2 .
[0030] First, 1000-3000A of oxidation silicon film 102 is preferably formed in thickness of 1500-2500A as substrate film on an insulating substrate 101. A glass substrate or a quartz substrate is used as an insulating substrate. Moreover, the oxidation silicon film forms membranes by the plasma-CVD method using TEOS.
[0031] Next, 200-800A of amorphous silicon film which is not illustrated is preferably formed by the plasma-CVD method in thickness of 500-600A. And the amorphous silicon film is crystallized with laser or heat. Then, patterning of the crystallized silicon film is carried out, and the semi-conductor island fields 103 and 104 are formed. In addition, they are 1x1019 atom / cm3 about boron (B) to the amorphous silicon film at this time. You may add by concentration. Since this is performed in order to adjust the threshold (Vth) of a transistor, concentration is suitably adjusted in the above-mentioned range. It is good to add on the silicon film used as especially an N channel mold transistor.
[0032] And 800-2000A of oxidation silicon film is preferably formed in thickness of 1000-1500A as gate dielectric film 105. This oxidation silicon film forms membranes by the plasma-CVD method using the mixture of gas of a silane and a nitrogen monoxide. Moreover, the layered product of silicon nitride or oxidation silicon, and silicon nitride may be used as gate dielectric film. In this way, the condition of drawing 1 (A) is acquired.
[0033] Next, the aluminum film which is not illustrated on gate dielectric film 105 is formed by the spatter. In order to prevent that a hillock and a whisker occur to aluminum at a next heating process, it is good for this aluminum film to carry out little addition of a scandium, titanium, the silicon, etc. Moreover, a tantalum may be used instead of aluminum.
[0034] Then, using a tartaric acid, the front face of the aluminum film is anodized and a 100A very thin precise oxide film on anode is formed. This oxide film on anode is effective in improving the adhesion of a mask. And the resist mask which is not illustrated on a precise anodized film is arranged, patterning of the aluminum film and the precise anodized film is carried out, and the gate electrodes 106 and 107 are formed.
[0035] Next, using oxalic acid, the side face of the gate electrodes 106 and 107 is anodized, and the porosity oxide films on anode 108 and 109 are formed. And a resist mask is removed, again, a gate electrode is anodized using a tartaric acid, a gate electrode is enclosed, and the precise oxide films on anode 110 and 111 are formed. In this way, the condition of drawing 1 (B) is acquired.
[0036] If the condition of drawing 1 (B) is acquired, the ion implantation of Lynn (P) will be carried out into the semi-conductor island field 103 and 104 by using the gate electrodes 106 and 107 and oxide films on anode 108-111 as a mask. the dose at this time -- 9x1014 atom / [1x1014 -] cm2 -- 7x1014 atom / [2x1014 -] cm2, and acceleration voltage are preferably set to 80kV. This process is called a heavy dope to the process of next drawing 2 (F). In this way, n+ The mold impurity ranges 112-115 are formed. (Drawing 1 (C))
[0037] Then, the porosity oxide films on anode 108 and 109 are removed, and 0.3 micrometers or more of interlayer insulation films 116 are preferably formed in thickness of 0.5 micrometers or more. As an interlayer insulation film, the laminating of the laminating of a silicon nitride film, the oxidation silicon film, a silicon nitride film, and the oxidation silicon film, the organic resin film, a silicon nitride film, and the organic resin film, the laminating of the oxidation silicon film and the organic resin film, etc. can be used. If the laminating of a silicon nitride film and the organic resin film is used, the laminating which turned the silicon nitride film down and turned the organic resin film up can reduce organic contamination. Moreover, the same is said of the laminating of the oxidation silicon film and the organic resin film. Furthermore, it is more desirable to use inorganic substances, such as a laminating of a silicon nitride film, the oxidation silicon film, a silicon nitride film, and the oxidation silicon film, if organic substance contamination is suppressed to the minimum. In this way, the condition of drawing 1 (D) is acquired.
[0038] Next, patterning of the interlayer insulation film is carried out, and puncturing is opened on the semi-conductor island field 104 used as a P channel mold transistor. If the quick ingredient of an etching rate is used for the interlayer

insulation film 116 to gate dielectric film 105 at this time, gate dielectric film will serve as a stopper of etching. For example, it is good to use the oxidation silicon film for gate dielectric film, and to use the laminating of a silicon nitride film, the organic resin film or a silicon nitride film, and the organic resin film etc. for an interlayer insulation film. If it considers that organic substance contamination also mentioned above, it is more desirable to use the oxidation silicon film for gate dielectric film, and to use a silicon nitride film for an interlayer insulation film. Moreover, gate dielectric film may also be etched and etching may be stopped in a semi-conductor layer.

[0039] And the ion implantation of the boron (B) is carried out by using an interlayer insulation film as a mask. Since an interlayer insulation film has the thickness of 0.3 micrometers or more, it functions enough as a mask. Moreover, the dose at this time is made [more] than the dose which poured in Lynn in the process of drawing 1 (C). In this example, 5x1015 atom / [1x1015 -] cm2, and acceleration voltage are set to 65kV for a dose. Thus, since the dose of boron is larger than the dose of Lynn, it is reversed and the conductivity type of impurity ranges 114 and 115 serves as p mold impurity ranges (the source / drain field) 117 and 118. And 119 becomes the channel formation field of a P channel mold transistor. In this way, the condition of drawing 2 (E) is acquired.

[0040] And shortly, opening of the semi-conductor island field 105 top used as an N channel mold transistor is carried out, and Lynn (P) is poured in again. The dose of Lynn at this time is made smaller than the 1st dose of Lynn. In this example, a dose sets 5x1013 atom / [1x1013 -] cm2, and acceleration voltage to 80kV. This process is called a light dope to the process of drawing 1 (C).

[0041] It is n+ to the fields 120 and 121 to which Lynn was not poured in according to this process at the time of the 1st Lynn impregnation. Lynn is poured in by concentration lower than the mold impurity ranges 112 and 113. This n - The mold impurity ranges 120 and 121 are called a LDD field, ease electric-field concentration with a gate electrode and an impurity range, and are effective in reducing leakage current. Moreover, 122 becomes the channel formation field of an N channel mold transistor.

[0042] In addition, since the dose of this 2nd Lynn impregnation is smaller than the dose of boron impregnation, the conductivity type of p mold impurity ranges 117 and 118 is not reversed. In this way, the condition of drawing 2 (F) is acquired.

[0043] Then, a contact hole is formed in gate dielectric film 105, and the metal membrane which does not cover and illustrate a gate electrode and an interlayer insulation film is formed. As a metal membrane, the aluminum film and the cascade screen of aluminum and titanium can be used. And patterning of the metal membrane is carried out and the source / drain electrode, and wiring 123-125 are formed. Then, the passivation film 126 is formed.

[0044] In this way, a complementary-type thin film transistor can be formed. (Drawing 2 (G)) In addition, it sets to drawing 2 (F) and is n. - It is this n although the mold impurity ranges 120 and 121 are formed. - The mold impurity ranges 120 and 121 may be formed after the oxide film on anode 108 of the porosity of the process of drawing 1 (D), and 109 removal.

[0045] There is a characteristic thing in the semiconductor device which has the complementary-type thin film transistor formed as mentioned above to the transistor produced by the approach of the conventional example. This is explained using drawing 5 .

[0046] Since the interlayer insulation film is functioning [1st] as a mask at the time of impurity impregnation first, the impurity (Lynn and boron) is contained in the interlayer insulation film. The concentration is 1x1017 atom / cm3, respectively. It is above. Moreover, it is not only merely contained, but as shown in the right-hand side of drawing 5 (A), it is the distribution which has inclination in concentration along the direction of thickness, respectively. This shows that the ion implantation of the impurity was carried out to the interlayer insulation film. In addition, the value (1x1017 atom / cm3 above) of the concentration of the above-mentioned impurity shows the maximum of inclination.

[0047] Moreover, there is a peak in distribution of high impurity concentration, and the location of the peak changes with Lynn and boron. This is because dope conditions differ in each. Moreover, it changes also with a light dope and heavy dopes.

[0048] The 2nd interlayer insulation film is a point which forms puncturing on a transistor. That is, in drawing 5 (A), an interlayer insulation film 116 exists between the gate wiring 501, and a source (drain) electrode and wiring 125. However, an interlayer insulation film does not exist on a transistor. This is because the interlayer insulation film on a semi-conductor island field was removed, in order to dope an impurity in the semi-conductor island field 103 and 104.

[0049] It is the point which has a level difference in the neighborhood an interlayer insulation film, and a source electrode or a drain electrode touches [3rd] gate dielectric film. Drawing 5 (B) expands the part enclosed with 502 of drawing 5 (A). In this drawing, the level difference 503 is formed in gate dielectric film 105 in the neighborhood an interlayer insulation film 116 and the source (drain) electrode 125 touch. When patterning of the interlayer insulation film is carried out, over etching of this is carried out. Of course, over etching may not be carried out by conditions, such

as etching time.
[0050] Finally, when a resist is used for a doping mask, the resist layer may remain thinly on gate dielectric film. However, there is no above-mentioned resist layer on the gate dielectric film of the semiconductor device formed of this invention.
[0051] In addition, although this example showed the example in which the thin film transistor was formed on the insulating substrate, when forming a transistor in a semi-conductor substrate, it can form similarly. Moreover, the description on the structure of the produced semiconductor device is also as having explained above (drawing 11). In addition, in drawing 11 , 1101 is a semi-conductor substrate, 1102 is field oxide, and other parts are the same as the thin film transistor of this example.
[0052] [Example 2] This example is the production approach of the complementary-type thin film transistor of a bottom gate mold. The making process Fig. of this example is shown in drawing 6 and drawing 7 . Suppose that an N channel mold transistor is formed in left-hand side, and a P channel mold transistor is formed in right-hand side in drawing 6 and drawing 7 . Moreover, especially the production conditions that are not indicated are the same as an example 1.
[0053] First, the substrate film 602 is formed on an insulating substrate 601. Next, after [membrane formation] patterning of the aluminum film which is not illustrated is carried out, and the gate electrodes 603 and 604 are obtained. And the gate electrodes 603 and 604 are covered and gate dielectric film 605 is formed. Then, after [membrane formation] patterning of the semi-conductor layer which is not illustrated is carried out, and the semi-conductor island fields 606 and 607 are obtained. If the semi-conductor island fields 606 and 607 are obtained, an interlayer insulation film 608 will be formed. In this way, drawing 6 (A) is obtained.
[0054] Next, patterning of the interlayer insulation film is carried out, and a part of semi-conductor layer 609 and 610 used as a P channel mold transistor is exposed. And they are 5x1015 atom / [1x1015 -] cm2 about boron (B) ion to the semi-conductor layers 609 and 610 which used the interlayer insulation film as the mask and exposed it. It pours in with a dose and p mold impurity ranges (the source / drain field) 609 and 610 and the channel formation field 611 are formed. (Drawing 6 (B))
[0055] And patterning of the interlayer insulation film is carried out again, and a part of semi-conductor layer 612 and 613 used as a P channel mold transistor is exposed. then, the semi-conductor layers 612 and 613 which used the interlayer insulation film as the mask and exposed it -- the Lynn (P) ion -- 9x1014 atom / [1x1014 -] cm2 a dose -- pouring in -- n mold impurity ranges 612 and 613 (the source / drain field) -- 609, 610, and the channel formation field 614 are formed.
[0056] In addition, although Lynn is poured also into p mold impurity ranges 609 and 610 at this time, since there are few doses of Lynn than the dose of boron, the conductivity type of impurity ranges 609 and 610 is not reversed. In this way, the condition of drawing 6 (C) is acquired.
[0057] Then, after [membrane formation] patterning of the metal membrane which is not illustrated is carried out, and source wiring and the drain wiring 615-617 are formed. And the passivation film 618 is formed and the complementary-type thin film transistor of a bottom gate mold is obtained. (Drawing 7 (D))
[0058] In addition, as the example 1 explained to the interlayer insulation film of the semiconductor device produced in this example, the impurity (Lynn and boron) is contained and the concentration has become the distribution which has inclination along the direction of thickness.
[0059] [Example 3] In an example 1, a LDD field is formed using an oxide film on anode. This example explains how to form a LDD field with the LDD spacer formed in the both sides of a gate electrode using the interlayer insulation film. In addition, especially the making process and production conditions that are not indicated are the same as an example 1.
[0060] First, the semi-conductor island fields 803 and 804 are formed on substrate film top 802 formed on the insulating substrate 801. Then, gate dielectric film 805 is formed and the gate electrodes 806 and 807 are formed. (Drawing 8 (A))
[0061] Next, the light dope of Lynn (P) is performed by using the gate electrodes 806 and 807 as a mask. Conditions are made to be the same as that of the light dope of an example 1. In this way, n - The mold impurity ranges 808-811 are formed. (Drawing 8 (B))
[0062] Then, patterning of the interlayer insulation film 812 is carried out after forming an interlayer insulation film 812 (drawing 8 (C)), and puncturing is opened on the semi-conductor island field 804 used as a P channel mold transistor. Gate dielectric film is also etched in this example. Of course, etching may be stopped with gate dielectric film. And the ion implantation of the boron (B) is carried out by using an interlayer insulation film as a mask. This dope condition is the same as an example 1. At this time, a conductivity type is reversed and impurity ranges 810 and

811 serve as p mold. Moreover, the channel formation field 813 is formed. (Drawing 9 (D))
[0063] Next, opening of the semi-conductor island field 803 top used as an N channel mold transistor is carried out. A spacer 814 is formed in the both sides of the gate electrode 806 at this time. moreover -- and an interlayer insulation film and a spacer -- a mask -- carrying out -- again -- Lynn -- (P) is poured in. The conditions at this time are performed with the heavy dope of an example 1.
[0064] By this process, they are impurity ranges 815 and 816n. - It becomes the field where high impurity concentration is larger than the mold impurity ranges 817 and 818 (n+ mold impurity range). Therefore, impurity ranges 817 and 818 turn into a LDD field. Moreover, 819 is a channel formation field. (Drawing 9 (E))
[0065] Then, like an example 1, the source / drain wiring 820-822, and the passivation film 823 are formed, and a complementary transistor is formed.
[0066] In addition, although this example showed the example in which the thin film transistor was formed on the insulating substrate, when forming a transistor in a semi-conductor substrate, it can form similarly. Moreover, the description on the structure of the produced semiconductor device is also as having explained to the example 1. Furthermore, the impurity of Lynn and boron is contained in the spacer as well as an interlayer insulation film.
[0067] As mentioned above, since it is not necessary to form the film for LDD spacers specially and a contact hole is also formed in the case of LDD spacer formation, a process can be simplified. Moreover, the resist mask for doping is not used.
[0068] [Example 4] In drawing 5 , insulation may fully be unable to be taken only with the interlayer insulation film 116 between the source (drain) wiring 125 and the gate wiring 501. In this case, as shown in drawing 10 , the 2nd interlayer insulation film 1001 is formed on an interlayer insulation film 116. This example is applicable not only to the example 1 but an example 2 and an example 3.
[0069] As the 2nd interlayer insulation film, the oxidation silicon film, a silicon nitride film, organic resin film, or those laminatings can be used. Moreover, the impurity (Lynn and boron) is not contained in this 2nd interlayer insulation film like an interlayer insulation film 116.
[0070] [Example 5] This example explains the application product using the semiconductor device using this invention. There is a circumference circuit for driving a semiconductor integrated circuit (logical circuits, such as a CMOS circuit, a DRAM circuit, and a SRAM circuit) and a active-matrix mold electro-optic device etc. in the semiconductor device using this invention. Below, an example is given and explained about the application product.
[0071] Drawing 12 (A) is a cellular phone and consists of a body 2001, the voice output section 2002, the voice input section 2003, an indicating equipment 2004, an actuation switch 2005, and an antenna 2006. This invention is applicable to the integrated circuit built into the interior of the circumference circuit and equipment of a display 2004.
[0072] Drawing 12 (B) is a video camera and consists of a body 2101, an indicating equipment 2102, the voice input section 2103, an actuation switch 2104, a dc-battery 2105, and the television section 2106. This invention is applicable to the integrated circuit built into the interior of the circumference circuit and equipment of a display 2102.
[0073] Drawing 12 (C) is a mobile computer and consists of a body 2201, the camera section 2202, the television section 2203, an actuation switch 2204, and a display 2205. This invention is applicable to the integrated circuit built into the interior of the circumference circuit and equipment of a display 2205.
[0074] Drawing 12 (D) is a head MAUN ten display, and consists of a body 2301, an indicating equipment 2302, and the band section 2303. This invention is applicable to the integrated circuit built into the interior of the circumference circuit and equipment of a display 2302.
[0075] Drawing 12 (E) is a rear mold projector, and consists of a body 2401, the light source 2402, an indicating equipment 2403, a polarization beam splitter 2404, reflectors 2405 and 2406, and a screen 2407. This invention is applicable to the integrated circuit built into the interior of the circumference circuit and equipment of a display 2403.
[0076] Drawing 12 (F) is a front mold projector, and consists of a body 2501, the light source 2502, a display 2503, optical system 2504, and a screen 2505. This invention is applicable to the integrated circuit built into the interior of the circumference circuit and equipment of a display 2503.
[0077] The semiconductor device using this invention above else can be used also for application products, such as a personal computer and a personal digital assistant device. Thus, the semiconductor device using this invention is crossed to the large range, and can be used.
[0078]
[Effect of the Invention] The resist mask for doping can be lost by using an interlayer insulation film as a mask in a doping process. Thereby, organic substance contamination of a semiconductor device can be reduced. Moreover, a making process can be simplified.
[0079] Furthermore, if an interlayer insulation film is used as a LDD spacer, a LDD field can be formed at the

simplified process.

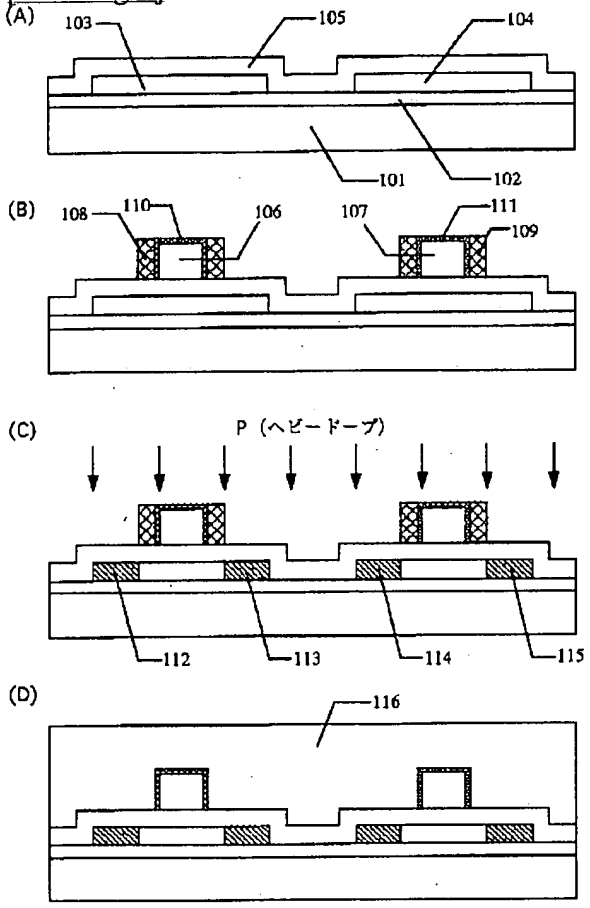
[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

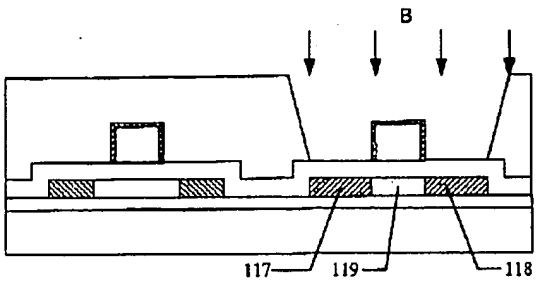
DRAWINGS

[Drawing 1]

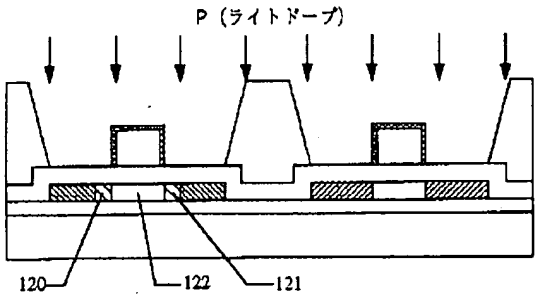


[Drawing 2]

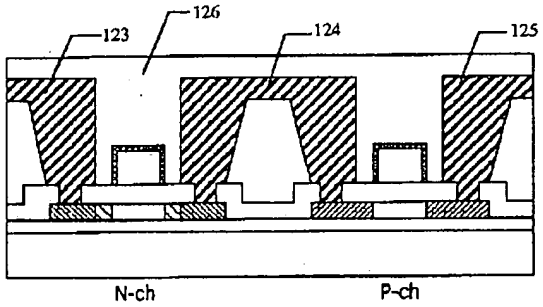
(E)



(F)

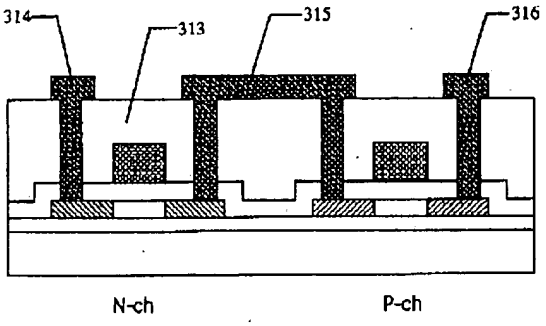


(G)



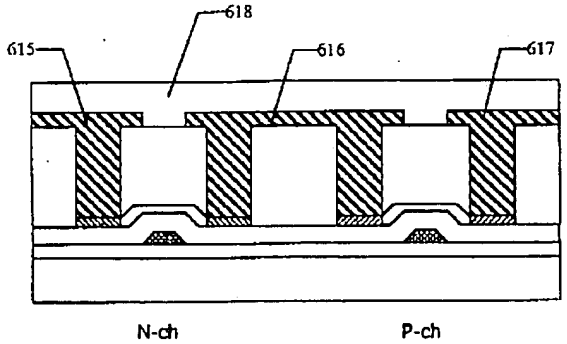
[Drawing 4]

(D)



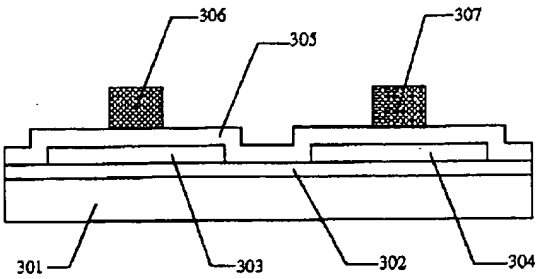
[Drawing 7]

(D)



[Drawing 3]

(A)



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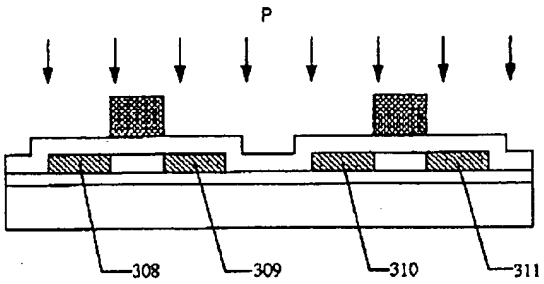
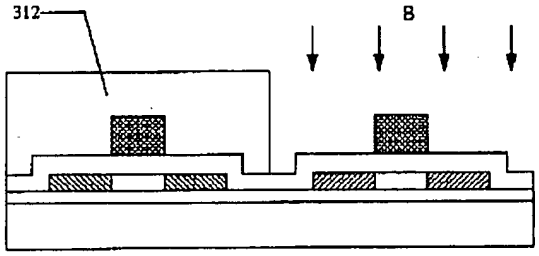
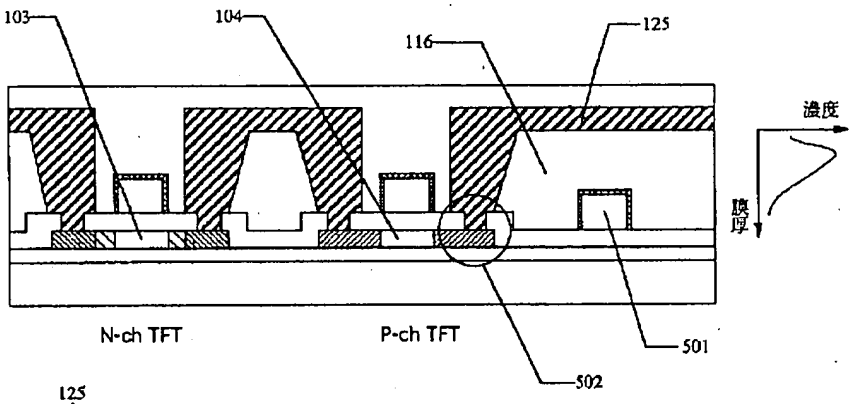


(C)



[Drawing 5]

(A)



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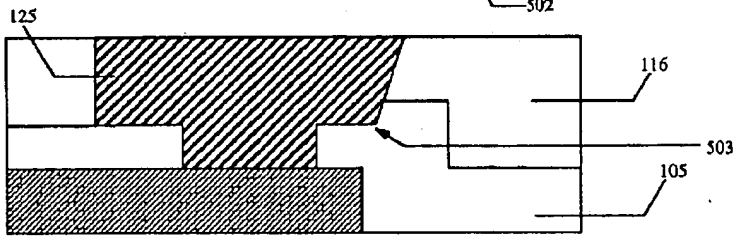
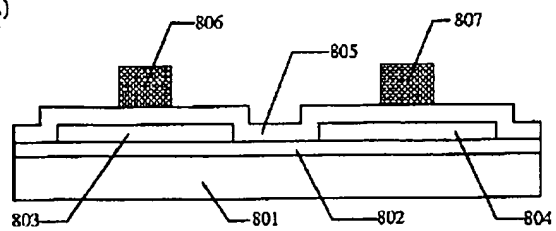


[Drawing 8]

(A)



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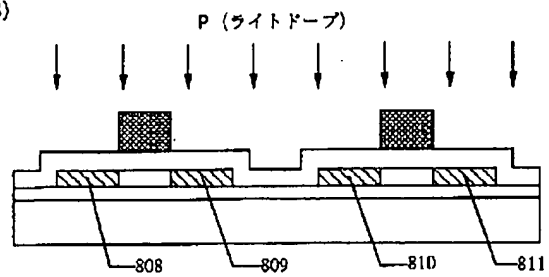

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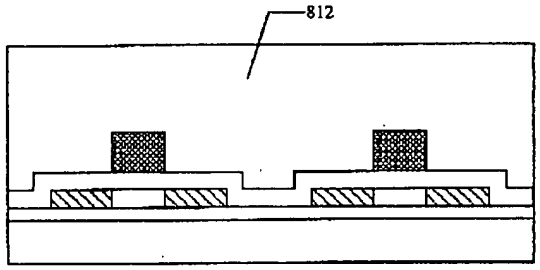
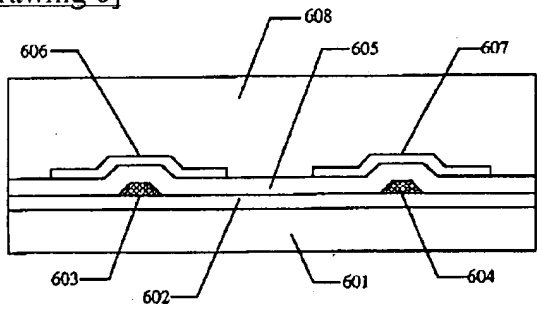


[Drawing 6]

(A)



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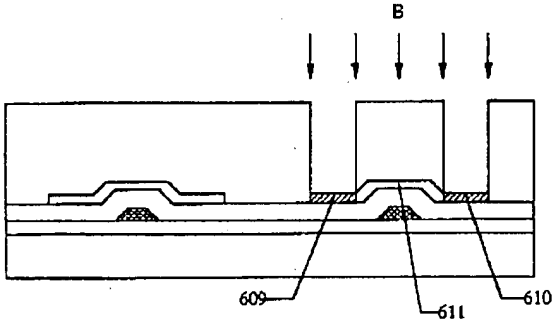

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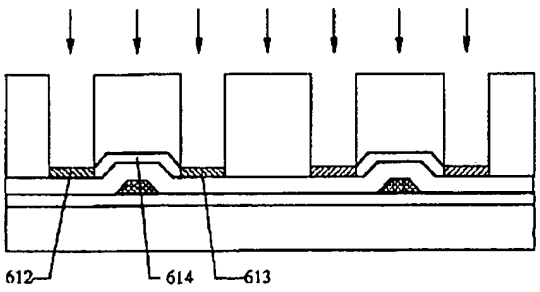
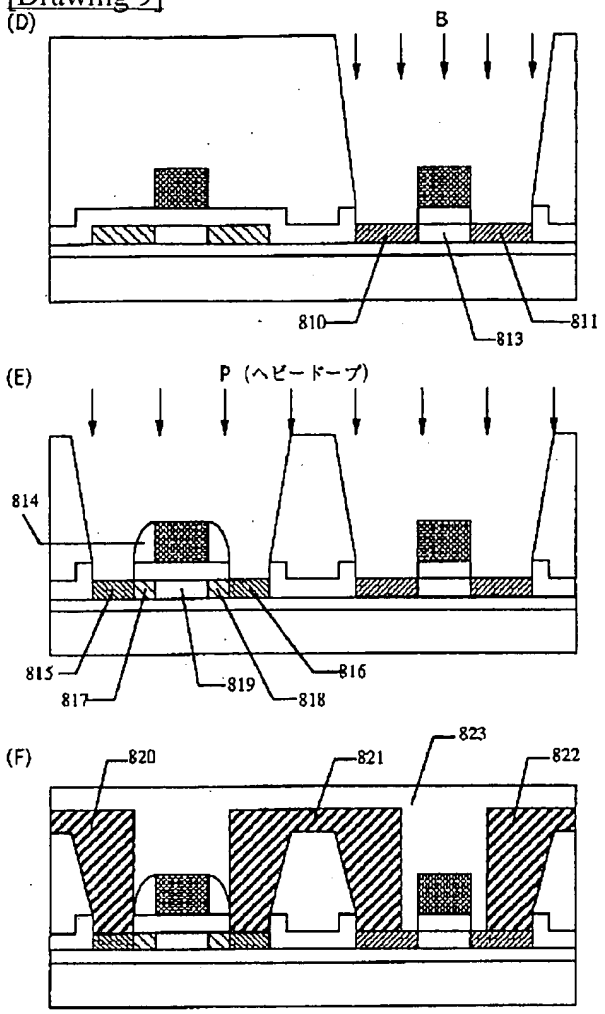
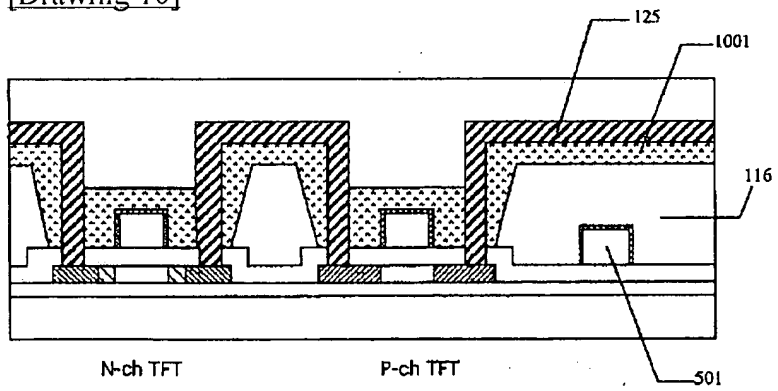


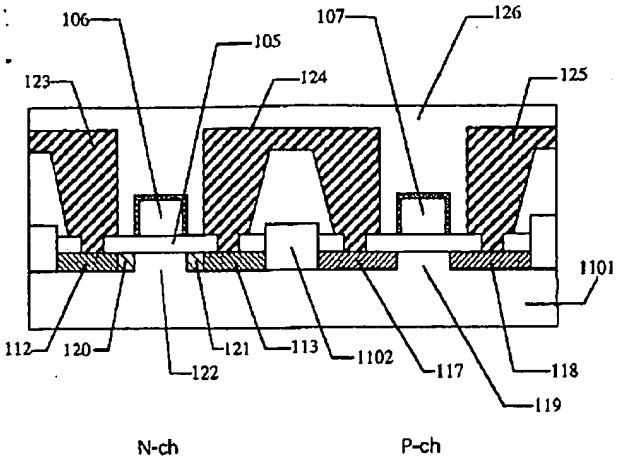
[Drawing 9]



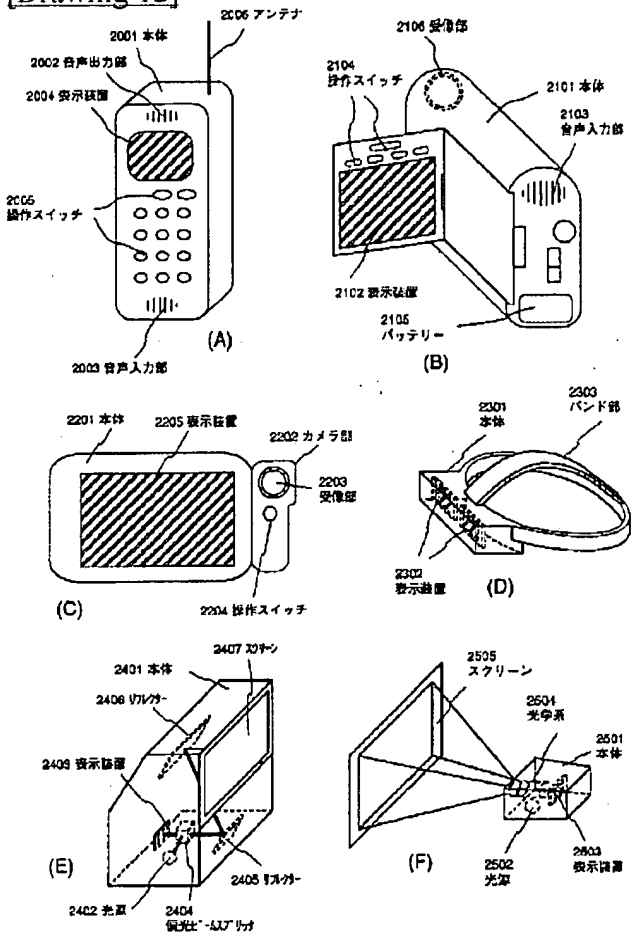
[Drawing 10]



[Drawing 11]



[Drawing 12]



[Translation done.]

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The process which forms at least two semi-conductor island fields on an insulating substrate, and the process which forms gate dielectric film on said semi-conductor island field, The process which forms a gate electrode on said gate dielectric film, and said gate electrode are used as a mask. The process which pours in the 1st impurity all over said semi-conductor island field, and the process which covers said gate dielectric film and said gate electrode, and forms an interlayer insulation film, The process which carries out patterning of said interlayer insulation film, and exposes at least one of said gate electrodes, The production approach of the semiconductor device characterized by having the process which pours in the 2nd impurity all over the semi-conductor island field under said exposed gate electrode by using said gate electrode and said interlayer insulation film as a mask.
[Claim 2] The process which forms gate dielectric film on a semi-conductor substrate, and the process which forms at least two gate electrodes on said gate dielectric film, The process which pours in the 1st impurity into said semi-conductor by using said gate electrode as a mask, The process which covers said gate dielectric film and said gate electrode, and forms an interlayer insulation film, The production approach of the semiconductor device which carries out patterning of said interlayer insulation film, and is characterized by having the process which exposes at least one of said gate electrodes, and the process which pours in the 2nd impurity into said semi-conductor by using said gate electrode and said interlayer insulation film as a mask.
[Claim 3] The process which forms at least two gate electrodes on an insulating substrate, and the process which forms gate dielectric film on said gate electrode, The process which forms at least two semi-conductor layers on said gate dielectric film, The process which forms an interlayer insulation film on said semi-conductor layer, and the process which carries out patterning of said interlayer insulation film, and exposes a part of at least one semi-conductor layer among said semi-conductor layers, The process which carries out patterning of said interlayer insulation film to the process which pours in the 1st impurity into said exposed semi-conductor layer by using said interlayer insulation film as a mask, and exposes a part of semi-conductor layer of others [layer / said / which was exposed / semi-conductor], The production approach of the semiconductor device characterized by having the process which pours in the 2nd impurity into said all semi-conductor layers by using said interlayer insulation film as a mask.
[Claim 4] The process which forms a semi-conductor island field on an insulating substrate, and the process which forms gate dielectric film on said semi-conductor island field, The process which forms a gate electrode on said gate dielectric film, and said gate electrode are used as a mask. The process which pours in a low-concentration impurity all over said semi-conductor island field, and the process which covers said gate dielectric film and said gate electrode, and forms an interlayer insulation film, The production approach of the semiconductor device characterized by having the process which etches said interlayer insulation film and forms a spacer in the side face of a gate electrode, and the process which pours in a high-concentration impurity all over said semi-conductor island field by using said gate electrode and said spacer as a mask.
[Claim 5] The process which forms gate dielectric film on a semi-conductor substrate, and the process which forms a gate electrode on said gate dielectric film, The process which pours in a low-concentration impurity into said semi-conductor by using said gate electrode as a mask, The process which covers said gate dielectric film and said gate electrode, and forms an interlayer insulation film, The production approach of the semiconductor device characterized by having the process which etches said interlayer insulation film and forms a spacer in the side face of a gate electrode, and the process which pours in a high-concentration impurity into said semi-conductor by using said gate electrode and said spacer as a mask.
[Claim 6] In the semiconductor device which has at least one P channel mold transistor and at least one N channel mold transistor Said P channel mold transistor and said N channel mold transistor, respectively A channel formation field, a

source field, and a drain field, The gate electrode formed in the neighborhood of said channel formation field through gate dielectric film, The source wiring electrically connected to said source field, and drain wiring electrically connected to said drain field, It has the interlayer insulation film formed in the bottom of said source wiring or said drain wiring. To said interlayer insulation film The semiconductor device characterized by adding the same impurity as the impurity added by the source field and drain field of said P channel mold transistor or said N channel mold transistor.

[Claim 7] The concentration of the impurity added by said interlayer insulation film in claim 6 is a semiconductor device characterized by being the distribution which has inclination in the direction of thickness of said interlayer insulation film.

[Claim 8] It is the semiconductor device characterized by the thickness of said interlayer insulation film being 0.3 micrometers or more in claim 6 thru/or 7.

[Claim 9] It is the semiconductor device characterized by said interlayer insulation film consisting of an inorganic substance in claim 6 thru/or 8.

[Claim 10] In the semiconductor device which has at least one P channel mold transistor and at least one N channel mold transistor Said P channel mold transistor and said N channel mold transistor, respectively A channel formation field, a source field, and a drain field, The gate electrode formed in the neighborhood of said channel formation field through gate dielectric film, Gate wiring electrically connected to said gate electrode, and the source wiring electrically connected to said source field, Drain wiring electrically connected to said drain field, and the 1st interlayer insulation film formed on said gate wiring, It has said source wiring or said drain wiring, and the 2nd interlayer insulation film formed between said 1st interlayer insulation film. To said 1st interlayer insulation film The semiconductor device characterized by adding the same impurity as the impurity added by the source field and drain field of said P channel mold transistor or said N channel mold transistor.

[Claim 11] The concentration of the impurity added by said 1st interlayer insulation film in claim 10 is a semiconductor device characterized by being the distribution which has inclination in the direction of thickness of said interlayer insulation film.

[Claim 12] It is the semiconductor device characterized by the thickness of said 1st interlayer insulation film being 0.3 micrometers or more in claim 10 thru/or 11.

[Claim 13] It is the semiconductor device characterized by said 1st interlayer insulation film consisting of an inorganic substance in claim 10 thru/or 12.

[Claim 14] In the semiconductor device which has at least one P channel mold transistor and at least one N channel mold transistor Said P channel mold transistor and said N channel mold transistor, respectively A channel formation field, a source field, and a drain field, The gate electrode formed in the neighborhood of said channel formation field through gate dielectric film, The source wiring connected to the source electrode connected to said source field at said source electrode, It has the drain electrode connected to said drain field, and the interlayer insulation film formed in the bottom of drain wiring connected to said drain electrode, said source wiring, or said drain wiring. To said gate dielectric film Said interlayer insulation film, The semiconductor device characterized by a level difference being in the neighborhood said source electrode or a drain electrode touches.

[Claim 15] At least one P channel mold transistor and at least one N channel mold transistor, Gate wiring electrically connected to the gate electrode of said P channel mold transistor or said N channel mold transistor, The source wiring electrically connected to the source field of said P channel mold transistor or said N channel mold transistor, Drain wiring electrically connected to the drain field of said P channel mold transistor or said N channel mold transistor, The semiconductor device characterized by having the interlayer insulation film prepared between said gate wiring, and said source wiring or said drain wiring, and carrying out opening of said interlayer insulation film on said P channel mold transistor and said N channel mold transistor.

[Claim 16] The semiconductor device characterized by the same impurity as the impurity added by the source field and drain field of said P channel mold transistor or said N channel mold transistor being added by said interlayer insulation film in claim 14 thru/or 15.

[Claim 17] The concentration of the impurity added by said interlayer insulation film in claim 16 is a semiconductor device characterized by being the distribution which has inclination in the direction of thickness of said interlayer insulation film.

[Claim 18] It is the semiconductor device characterized by the thickness of said interlayer insulation film being 0.3 micrometers or more in claim 14 thru/or 17.

[Claim 19] It is the semiconductor device characterized by said interlayer insulation film consisting of an inorganic substance in claim 14 thru/or 18.

[Translation done.]